IN THE CLAIMS

Please add new Claims 25-32 as follows:

25. The method of Claim 1, wherein at least one of said plurality of instruction words comprises an op-code and a plurality of fields, each of said fields comprising a plurality of bits, said at least one instruction word being encoded according to the method comprising:

associating a first of said fields with a first data source;

associating a second of said fields with a second data source; and

performing a logical operation using said first and second data sources as operands, said logical operation being specified by said op-code.

26. The method of Claim 1, further comprising generating a long immediate constant using a single word instruction according to the method comprising:

providing an instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits;

selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

storing said shifted immediate value in a register.

27. The method of Claim 25, wherein said plurality of instruction words further comprises at least one instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits, said at least one instruction word with short immediate value being used to generate a long immediate constant according to the method comprising:

selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

storing said shifted immediate value in a register.

28. The method of Claim 27, wherein said at least one instruction word having a plurality of fields and said at least one instruction word having a short immediate value comprise the same instruction word(s).

29. The digital processor of Claim 14, wherein said wherein at least one of said plurality of instruction words comprises an op-code and a plurality of fields, each of said fields comprising a plurality of bits, said at least one instruction word being encoded by:

associating a first of said fields with a first data source;

associating a second of said fields with a second data source; and

performing a logical operation using said first and second data sources as operands, said logical operation being specified by said op-code.

30. The digital processor of Claim 14, wherein said processor is further adapted to generate a long immediate constant using a single word instruction by:

providing an instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits;

selecting a portion of said plurality of bits of said at least one short immediate value;

shifting all of said bits of said at least one short immediate value using said op-code and only said portion of bits to produce a shifted immediate value; and

storing said shifted immediate value in a register.

31. The digital processor of Claim 29, wherein said plurality of instruction words further comprises at least one instruction word having an op-code and at least one short immediate value associated therewith, said at least one short immediate value comprising a plurality of bits, said at least one instruction word with short immediate value being used to generate a long immediate constant according to the method comprising:

selecting a portion of said plurality of bits of said at least one short immediate value;